REMARKS

Claims 1-21 are now pending in the application. Claims 7, 8 and 19 have been indicated as allowable. Applicants would like to thank the Examiner for courtesy extended during the Examiner Interview with Mr. Donald Daley. The amendments to the claims contained herein are of equivalent scope as originally filed and, thus, are not a narrowing amendment. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

DRAWINGS

The gain of the opamps in FIGs. 2-5 and 7-11 have been amended to $-g_m$ to correct typographical errors in the drawings and to make the drawings consistent with the nesting concept that was described in the specification and claims. In particular, the additional levels of nesting involve inserting one TIA within another. The polarity of the gain parameter g_m of each of the nested TIA stages remains negative (as shown in FIG. 1). No new matter has been presented.

REJECTION UNDER 35 U.S.C. § 103

Claims 1, 9, 14-16, 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuyama (JP406061752A) in view of Holt "Electronic Circuits Digital and Analog". This rejection is respectfully traversed.

Neither Matsuyama nor Holt show, teach or suggest a nested transimpedance amplifier (TIA) that is recited in Claim 1. Matsuyama inserts additional components within a zero order TIA. However, Claim 1 recites a zero order TIA that is inserted or

nested within other components, specifically an opamp and feedback resistance. Claim 1 is allowable for this reason.

Applicants are submitting herewith a translation of Matsuyama. As best understood by Applicants, Matsuyama describes a prior art zero order TIA in conjunction with FIG. 5 thereof. **See ¶ 0002-5 of Matsuyama**. The zero order TIA includes a feedback resistance 3 and an inverting amplifier 2. Id. All the embodiments in Matsuyama have the same feedback resistance 3, which forms part of the zero order TIA. **See e.g., FIGs. 1-6 of Matsuyama.**

Matsuyama inserts additional components in the loop containing the feedback resistance 3 of the zero order TIA. For example, in FIG. 1, the transistor 4, the impedance control amplifier 6 and the additional inverting amplifiers 2-2 and 2-3 are inserted in the loop containing the feedback resistance 3. **See ¶ 0013-14 of Matsuyama.** In contrast, in one exemplary embodiment shown in FIG. 7 of Applicant's invention, it can be seen that the exemplary zero order TIA (including amplifiers 415 and 425 and feedback resistance 420) is nested or inserted within the opamp 710 and the feedback resistance 715.

Matsuyama describes several problems with the zero order TIA in FIG. 5. **See ¶ 0004 of Matsuyama.** When the current I increases, V_{out} of the amplifier 2 in FIG. 5 saturates, which limits the dynamic range of the TIA circuit. Id. In one prior art solution described by Matsuyama in conjunction with FIG. 6, the amplifier 2 is replaced by inverting amplifiers 2-1, 2-2, and 2-3. **See ¶ 0006-7 of Matsuyama.** Therefore, Matsuyama inserted two additional cascaded inverting amplifiers in the loop containing the feedback resistance of the zero order TIA.

Next, a variable impedance feedback transistor 4 was added at the input and output of the first inverting amplifier 2-1. Id. This transistor 4 is also inserted in the loop containing the feedback resistance 3 of the zero order TIA. **See FIG. 6 of Matsuyama.** An automatic gain control (AGC) circuit 5 provides feedback to the gate of the variable impedance feedback transistor 4. **See ¶ 0007 of Matsuyama.** As the current I increases, the AGC 5 provides feedback to the transistor 4, which increases the current through the transistor 4 and reduces the current flowing to the feedback resistance 3. Id. The problem with this arrangement according to Matsuyama is the slow response time of the feedback from AGC 5 to the variable impedance feedback transistor 4. **See ¶ 0008 of Matsuyama.**

To reduce the response time of the variable impedance feedback transistor 4, Matsuyama added the impedance control amplifier 6 and removed the AGC circuit 5 as shown in FIG. 1. **See ¶ 0013 of Matsuyama.** This amplifier 6 is also inserted in the loop containing the feedback resistance 3 of the zero order TIA. **See FIG. 1 of Matsuyama.** As the current I increases at the output of the first stage 2-1, the impedance control amplifier 6 increases drive to the gate of the variable impedance feedback transistor 4. **See ¶ 0017 of Matsuyama.** This lowers the impedance of the variable impedance feedback transistor 4, which reduces current to the feedback resistance 3 and increases the current through the variable feedback transistor 4. Id.

While Matsuyama inserts additional components within a zero order TIA, Claim 1 requires something completely different. Claim 1 recites a zero order TIA that is inserted or nested within other components (the feedback resistance and the opamp).

Specifically, the body of Claim 1 defines a zero order TIA having an input and an output. The zero order TIA is nested with a first opamp and a feedback resistance. More specifically, the first opamp has an input that communicates with an output of the zero order TIA. The feedback resistance has one end that communicates with the input of the zero order TIA and an output that communicates with an output of the first opamp. Therefore, Matsuyama does not meet the language of Claim 1 for this reason.

Matsuyama also does not meet the language of Claim 1 since the output of the amplifier 2-2 is not connected to the feedback resistance 3 (which is also connected to the input of a TIA). The output of the amplifier 2-2 is connected to the input of the amplifier 2-3. **See FIGs. 1 and 6 of Matsuyama.** The output of the amplifier 2-3 is connected to the feedback resistor 3. Id. This cascade arrangement of the amplifiers 2-2 and 2-3 may provide lower bandwidth than the nested arrangement disclosed by Applicants.

As a result of the foregoing differences, Applicants believe that Claim 1 is allowable over the prior art of record. Claims 2-6 and 9-12 depend directly or indirectly on Claim 1 and are allowable for the same reasons.

Neither Matsuyama nor Holt show, teach or suggest a nested differential mode transimpedance amplifier (TIA) as set forth in Claim 14. As set forth above, Matsuyama inserts additional components within a (non-differential mode) zero order TIA. Claim 14 recites a differential mode zero order TIA that is inserted or nested within additional components including opamps and feedback resistances.

As a result of the foregoing differences, Applicants believe that Claim 14 is also allowable over the prior art of record. Claims 15-18 and 20-21 depend directly or indirectly on Claim 14 and are allowable for the same reasons.

ALLOWABLE SUBJECT MATTER

Applicants would like to thank the Examiner for favorable consideration of Claims 7, 8 and 19, which were indicated as allowable if rewritten in independent form. At the end of prosecution, Applicants intend to rewrite Claims 7, 8 and 19 into independent form if needed.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1211.

Respectfully submitted,

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By: _____
Michael D. Wiggins
Reg. No. 34,754

MARVELL SEMICONDUCTOR, INC.
700 FIRST AVENUE, MAIL STOP 509
SUNNYVALE, CA 94089
408-222-2500